IN THE CLAIMS:

Please substitute the following amended claims for their corresponding claims:

1. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry, wherein the slurry modifier polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the modifier-contained slurry.

5. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding a slurry modifier to the slurry, wherein the slurry modifier polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the modifier-contained slurry.

8. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding ethylene glycol at a concentration of up to 50% for polishing low structure areas at a substantially zero rate and polishing high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the slurry.

10. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate such that the silicon dioxide forms low structure areas and high structure areas;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry to produce a modified slurry that polishes the low structure areas at a substantially zero rate and polishes the high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide having high structure areas and low structure areas using the modified slurry, whereby high

structure areas are polished at a rate approximating a blanket polishing rate and low structure areas are polished at a substantially zero rate.

13 (Twice Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate such that the silicon dioxide forms low structure areas and high structure areas;

forming a CMP slurry having a high structure polishing rate lower than a blanket polishing rate;

adding a slurry modifier to the slurry to produce a modified slurry that polishes high structures at a rate approximating the blanket polishing rate; and

polishing the high structure areas of silicon dioxide.

16. (Amended). A method of chemically-mechanically polishing a silicon dioxide layer having high structure areas and low structure areas overlying a semiconductor substrate consisting essentially:

forming a slurry comprising cerium oxide and ethylene glycol; and

polishing the silicon dioxide layer only such that the high structure areas are polished at a rate approximating a blanket polishing rate, and the low structure areas are polished at a substantially zero rate.

Attachment to Preliminary Amendment Accompanying Response to Office Action Under 37 C.F.R. § 1.111 Dated November 13, 2001

Claims Pending in Application Serial No. 09/270,606 Incorporating All Changes as of November 13, 2001

1. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry, wherein the slurry modifier polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the modifier-contained slurry.

2. The method of claim 1 wherein said forming includes setting a cerium oxide concentration of between about 1% and 50% by weight.

3. The method of claim 1 wherein said polishing includes CMP at a pressure of between about five psi and ten psi.

4. The method of claim 1 wherein said adding includes adding ethylene glycol at a concentration of up to 50%.

5. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding a slurry modifier to the slurry, wherein the slurry modifier polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the modifier-contained slurry.

6. The method of claim 5 wherein said polishing includes CMP at a pressure of between about five psi and ten psi.

7. The method of claim 5 wherein said adding includes adding ethylene glycol at a concentration of up to 50%.

8. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding ethylene glycol at a concentration of up to 50% for polishing low structure areas at a substantially zero rate and polishing high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide using the slurry.

9. The method of claim 8 wherein said polishing includes CMP at a pressure of between about five psi and ten psi.

10. (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate such that the silicon dioxide forms low structure areas and high structure areas;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry to produce a modified slurry that polishes the low structure areas at a substantially zero rate and polishes the high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide having high structure areas and low structure areas using the modified slurry, whereby high structure areas are polished at a rate approximating a blanket polishing rate and low structure areas are polished at a substantially zero rate.

11. The method of claim 10, wherein the high structure areas and the low structure areas are both formed of silicon dioxide.

12. The method of claim 10, wherein the slurry modifier is ethylene glycol.

13 (Twice Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate such that the silicon dioxide forms low structure areas and high structure areas;

forming a CMP slurry having a high structure polishing rate lower than a blanket polishing rate;

adding a slurry modifier to the slurry to produce a modified slurry that polishes high structures at a rate approximating the blanket polishing rate; and

polishing the high structure areas of silicon dioxide.

14. The method of claim 13, wherein the CMP slurry comprises cerium oxide.

15. The method of claim 13, wherein the slurry modifier is ethylene glycol.

16. (Amended). A method of chemically-mechanically polishing a silicon dioxide layer having high structure areas and low structure areas overlying a semiconductor substrate consisting essentially:

forming a slurry comprising cerium oxide and ethylene glycol; and

polishing the silicon dioxide layer only such that the high structure areas are polished at a rate approximating a blanket polishing rate, and the low structure areas are polished at a substantially zero rate.

17 (Amended). A method of fabricating an integrated circuit using CMP consisting essentially of:

providing a substrate;

depositing silicon dioxide over the substrate such that the silicon dioxide forms low structure areas and high structure areas;

forming a CMP slurry having a low-density high structure polishing rate and a high-density high structure polishing rate, wherein the low-density high structure polishing rate is essentially the same as a high-density high structure polishing rate; and

polishing the high structure areas, whereby the polishing rate is independent of pattern density.

18 The method of claim 17, wherein said forming includes setting a cerium oxide concentration of between about 1% and 50% by weight.

19. The method of claim 17, wherein said polishing includes CMP at a pressure of between about five psi and ten psi.

20. The method of claim 17, wherein said forming includes adding ethylene glycol at a concentration of up to 50%.